LEARNING OUTCOMES–BASED CURRICULUM FRAME WORK (LOCF)

In the

POST GRADUATE PROGRAMME
M.Sc., ELECTRONICS AND COMMUNICATION SYSTEMS

FOR THE STUDENTS ADMITTED FROM THE

ACADEMIC YEAR 2022-2023 AND ONWARDS

HINDUSTHAN EDUCATIONAL AND CHARITABLE TRUST

HICAS

HINDUSTHAN COLLEGE OF ARTS & SCIENCE (AUTONOMOUS)
(Affiliated to Bharathiar University and Accredited by NAAC)
COIMBATORE-641028
TAMILNADU, INDIA.
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INTRODUCTION

The students pursuing Electronics and Communication Systems course would develop in-depth understanding of various aspects of the subject. The working principles, design guidelines and experimental skills associated with different design methodologies for digital and embedded systems, communication electronics and control systems and various applications of electronic devices, circuits and systems are among such important aspects.

PREAMBLE

Learning Outcome Based Curriculum Framework for Master of Science (M.Sc.) in Electronics and Communication Systems is a post-graduation course. The credit system implemented through this curriculum, would allow students to develop a strong footing in the fundamentals and specialize in the disciplines of his/her liking and abilities.

VISION

To provide world class education to the students to face global challenges and to inculcate the latest trends in technological advancement. To cater the needs of the environmental and ethical values in the mind of students to become good citizens and entrepreneurs.

MISSION

The Mission of the college is to pursue a philosophy of perpetual acquisition of knowledge. The important policy is to provide value-based education and to bring out the hidden potentials in students that equip them to approach life with optimism.

PROGRAMME EDUCATIONAL OBJECTIVES (PEO)

PEO 1: Have a successful career in electronics academia/industries/entrepreneurs.

PEO 2: Critically analyze existing literature in an area of specialization.

PEO 3: Ethically develop innovative and research-oriented methodologies to solve the problems identified.

PEO 4: Be receptive to new technologies and attain professional competence through lifelong learning such as advanced degrees, publications and other professional activities.

PEO 5: Communicate effectively and manage resources skillfully as members and leaders of the profession.

PROGRAMME OUTCOME (PO)

PO1: DISCIPLINARY KNOWLEDGE: Utilize the basic knowledge in mathematics, science and technology in Electronics and Communication field.

PO2: PROBLEM SOLVING AND ANALYSING: Identify, formulate and solve complex problems to achieve demonstrated conclusions using mathematical principles and science in Electronics and Communication field.

PO3: ENVIRONMENT SUSTAINABILITY AND ETHICS: Design system components that meet the requirement of public safety and offer solutions to the societal and environmental concerns.

PO4: MODERN TOOL USAGE: Construct, choose and apply the techniques, resources and modern tools required for Electronics and Communication systems applications.

PO5:CO-OPERATIVE TEAM WORK & COMMUNICATIVE SKILLS: Communicate the electronic activities to technical society for documentation and presentation.

PO6: SELF DIRECTED / LIFE LONG LEARNING: Demonstrate resourcefulness for contemporary issues and lifelong learning. Interpret the data pertaining to Electronics and Communication problems and arrive at valid conclusions.

PO7: ENHANCING RESEARCH CULTURE: Apply research-based knowledge to design and conduct experiments, analyze, synthesizes.

PROGRAMME SPECIFIC OUTCOME (PSO)

PSO1: Apply the fundamental concepts of electronics and communication systems to design a variety of components and systems for technology applications.

PSO2: Select and apply cutting-edge hardware and software tools to solve complex Electronics and Communication systems problems.

PSO3: Adapt the emerging Information and Communication Technologies (ICT) to innovate ideas and solutions to existing/novel problems.

PSO4: Realize the fact that the knowledge and techniques learnt in this course has direct implication for the betterment of society and its sustainability.

PSO5: Analyze the functional characteristics of various concepts such as signal processing, image processing, communication, networking, embedded systems, VLSI and control system.

HINDUSTHAN COLLEGE OF ARTS & SCIENCE (AUTONOMOUS),

COIMBATORE-641028

SCHEME OF EXAMINATIONS - CBCS & LOCF PATTERN

(For the Students admitted from the Academic year 2022-2023 and Onwards)

PG PROGRAMME

Programme: M.Sc., **Branch: Electronics and Communication Systems**

Course Code	Course Type	Course Title	Credit points	Lecture Hours/ Week		Exam Duration (hours)	MAX. MARKS		
				Theory	Practical		I.E.	E.E	Total
		Semester – I							
22ELP01	DSC	Digital and Network Communication	4	5	-	3	50	50	100
22ELP02	DSC	Microwave and RADAR Navigation System	4	5	-	3	50	50	100
22ELP03	DSC	8051 Microcontroller with C Programming	4	5	-	3	50	50	100
22ELP04	DSC	Power Electronics	4	4	-	3	50	50	100
22ELP05	DSC	Practical I - Digital Communication Systems	3	-	5	5	50	50	100
22ELP06	DSC	Practical II - 8051Microcontroller And its Applications	3	-	5	5	50	50	100
22ELP07	SEC	Internship / Institutional Training / Mini-Project	2	-	-	-	100	-	100
22ELPE01	AEE	Open Elective – I	2	3	-	3	100	-	100
22ELPV01	ACC	VAC–I	1*	2	-	2	50	-	50**
22ELPJ01	SEC	Aptitude / Placement Training	Grade*	2	-	2	50	-	50**
-	SEC	SDR – Student Development Record	Assessment will be done in the end of III – rd semester						
		Total	**26**	**26**	**10**	-	**500**	**300**	**800**
		Semester – II							
22ELP08	DSC	Optical Fiber Communication	4	5	-	3	50	50	100
22ELP09	DSC	MEMS and Control Systems	4	5	-	3	50	50	100
22ELP10	DSC	Embedded Systems and RTOS	4	5	-	3	50	50	100
22ELP11	DSC	Modern VLSI Design	4	4	-	3	50	50	100
22ELP12	DSC	Practical III - Optical and Microwave Communication	3	-	5	5	50	50	100
22ELP13	DSC	Practical IV- Embedded System and RTOS	3	-	5	5	50	50	100
22ELP14	SEC	Internship / Institutional Training / Mini-Project /	2	-	-	-	100	-	100

		Extension Activity							
22ELPE02	AEE	Open Elective – II	2	3	-	3	100	-	100
22ELPV02	ACC	VAC–II	1*	2	-	2	50	-	50**
22ELPJ02	SEC	Online Courses	Grade*	-	-	-	-	-	C/NC
22ELPJ03	SEC	Aptitude / Placement Training	Grade*	2	-	2	50	-	50**
		Total	**26**	**26**	**10**	-	**500**	**300**	**800**
		Semester – III							
22ELP15	DSC	Mobile Communication	4	5	-	3	50	50	100
22ELP16	DSC	Digital Signal Processing	4	4	-	3	50	50	100
22ELP17	DSC	VLSI Programming	4	4	-	3	50	50	100
22ELP18	DSE	Elective–I / **DSE-I**	3	3	-	3	50	50	100
22ELP19	DSE	Elective–II / **DSE-II**	3	3	-	3	50	50	100
22ELP20	DSC	Practical V - Digital Signal Processing	3	-	5	5	50	50	100
22ELP21	DSC	Practical VI –VLSI Design	3	-	5	5	50	50	100
22ELP22	SEC	Internship / Institutional Training / Mini-Project / Extension Activity	2	-	-	-	100	-	100
22ELPE03	AEE	Open Elective–III	2	3	-	3	100	-	100
22ELPV03	ACC	VAC–III	1*	2	-	2	50	-	50**
22ELPJ04	SEC	Online Courses	Grade*	-	-	-	-	-	C/NC
22ELPJ05	SEC	Aptitude / Placement Training	Grade*	2	-	2	50	-	50**
22ELPJ06	SEC	SDR – Student Development Record	2*	-	-	-	-	-	-
		Total	**28**	**26**	**10**	-	**550**	**350**	**900**
		Semester – IV							
22ELP23	DSE	Elective-III/ **DSE-III**	3	5	-	3	50	50	100
22ELP24	DSE	Elective–IV / **DSE-IV**	3	5	-	3	50	50	100
22ELP25	DSC	Self-Study Course	3	-	-	3	50	50	100
22ELP26	SEC	Project Work /Student Research	5	-	-	-	100	100	200
Total			**14**	**10**	-	-	**250**	**250**	**500**
Grand Total			**94 +5 Extra Credit**				**1800**	**1200**	**3000 + (300**)**

- * denotes Extra credits which are not added with total credits.
- ** denotes Extra marks which are not added with total marks.
- VAC-Value Added Course (Extra Credit Courses)
- Grade -Grades depends on the marks obtained

Range of marks	Equivalent remarks
80 and above	Exemplary
70 – 79	Very good
60 – 69	Good
50 – 59	Satisfactory
Below 50	Not Satisfactory = NotCompleted

- **I.E**-Internal Exam
- **E.E**-External Exam
- **J**-Job Oriented Course
- **E**-Open Elective Papers

PASSING MINIMUM

- Passing Minimum for PG 50% (Both Internal and External)

Abstract for Scheme of Examination

(For the students admitted during the academic year 2022 - 2023 and onwards)

Course	Papers	Credit	Total Credits	Marks	Total Marks
Core /**DSC**	11	4	**44**	100	**1100**
Self-Study Course /**DSC**	1	3	3	100	**100**
Electives/**DSE**	4	3	**12**	100	**400**
Practical/ **DSC**	6	3	**18**	100	**600**
Project/ **SEC**	1	5	**5**	200	**200**
Internship/Institutional Training/Mini-Project / Extension Activity/SEC	3	2	**6**	100	**300**
Open Electives /**AEE**	3	2	**6**	100	**300**
Job Oriented Course / Value Added Course/SEC	3	1*	3*	50	**150****
Skill Based/ Placement/Aptitude **SEC**	3	Grade*	Grade*	50	**150****
Online Courses / SEC	**2**	Grade*	Grade*	-	-
SDR – SEC	**1**	2*	2*	-	-
Total			**94 + (5 Extra Credits)**		**3000 + (300**)**

List of Open Elective Papers	
Open Electives	Yoga for Human Excellence Human Health & Hygiene Indian Culture and Heritage Indian Constitution and Political System Consumer Awareness and Protection Professional Ethics and Human Values Human Rights, Women's Rights& Gender Equality Disaster Management Green Farming Campus to Corporate How to start a Business? Research Methodology and IPR General Studies for Competitive Examinations IIT JAM Examination (for Science only)
	Courses offered by the Departments to other Programmes

List of VAC/ JOC	
Value Added Courses(VAC)	Courses offered by the Departments (Additional credit Course)
	a) Electronic Test Instruments
	b) Verilog HDL
	c) Bioelectronics
	d) Materials Characterization
	e) IoT and its Applications
	f) Electric Vehicle Design
	g) Ocean Electronics
	h) Artificial Intelligence using Rasp berry Pi

Note: VAC / JOC courses can be added along with the above open electives

List of Elective Papers/ DSE (Can choose any one of the paper as electives)		
Electives/ **DSE-I**	Course Code	Title
	22ELP18A	Wireless Sensor Networks
	22ELP18B	RealTime System Design
Electives/ **DSE-II**	22ELP19A	ARM Core Processor
	22ELP19B	Virtual Instrumentation
Electives/ **DSE-III**	22ELP23A	Introduction to Robotics
	22ELP23B	Digital Circuits
Electives/ **DSE-IV**	22ELP24A	Introduction to Wireless and Cellular Communications
	22ELP24B	Design for Internet of Things

Syllabus Coordinator

Dr.R.PREMA

BOS-Chairman/Chairperson

Dr.K.THANGAVEL
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Academic Council – Member Secretary

PRINCIPAL

PRINCIPAL
Hindusthan College of Arts & Science (Autonomous),
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Coimbatore - 641 028.

PG Scheme of Evaluation (Internal & External Components)

(For the students admitted during the academic year 2022-2023 and onwards)

1. Internal Marks

Components	Marks
Test	15
Model Exam	15
Internal Assessment components	20 #
TOTAL	50

 # List of components for Internal Assessment

S.No	Components
1	Multiple choice questions
2	Video teach
3	Co-operative or Collaborative Learning
4	Mini Project/Assignment
5	Case study
6	Seminar
7	Role Play
8	Management Games

(Any four components from the above list with five marks each will be calculated .4x5=20 marks)

2. a) Components for Practical I.E.

Components	Marks
Test –I	15
Test - II	15
Observation	10
Application*	10
Total	50

b) Components for Practical E.E.

Components	Marks
Experiments/Exercise	40
Record	5
Viva	5
Total	50

3. Institutional/ Industrial Training, Mini Project and Major Project Work

Internships/Industrial Training (I.E)		Mini Project (I.E)	Major Project Work		
Component	**Marks**		**Component**	**Marks**	**Total Marks**
Work diary	25	-	I.E a)Attendance	20	
Report	50	50	b)Review	30	100
Viva-voce	25	50	c) Report	25	
			d)MocViva-Voce/ Presentation	25	
Total	100	100	E.E*		
			a) Final report	60	100
			b)Viva-voce	40	
				Total	200

*Evaluation of report and conduct of viva voce will be done jointly by Internal and External Examiners

4. Value Added Courses and Aptitude/Placement courses:

Components	Marks
Two Test (each 1 hour) of 25 marks each QP is objective pattern (25x1=25)	50
Total	50

5. Guideline for Open Elective

Two tests(each 2 hours) of 50 marks each [5 out of 8 descriptive type questions 5x10=50 Marks	Marks
	100

Guidelines:

1. The passing minimum for these items should be 50%
2. If the candidate fails to secure 50% passing minimum, he / she may have to reappear for the same in the Subsequent semesters
3. Item No's:4 is to be treated as 100% Internals and evaluation through online.
4. Item No.2: * - Application should be from the relevant practical subject other than the listed programmes. It must be enclosed in the practical record.

For all PG/MBA/MCA *Programmes* *(2022-2023Regulations)*

QUESTION PAPER PATTERN FOR CIA EXAM

Reg.No:---------- Q.P.CODE:

HINDUSTHAN COLLEGE OF ARTS & SCIENCE (AUTONOMOUS)

PG/MBA/MCA DEGREE CIA EXAMINATIONS ----------20--------

(----------Semester)

BRANCH: ----------

Subject Name: ----------

Time: Two Hours **Maximum: 50 Marks**

Section-A (4 x 4=16 Marks)

Answer **ALL** Questions

ALL questions carry **EQUAL** Marks

(Q.No: 1 to 4 Either Or type)

Section-B (3 x 8=24 Marks)

Answer any **THREE** Questions out of **FIVE** Questions

ALL questions carry **EQUAL** Marks

(Q.No: 5 to 9)

Section-C (1 x 10=10 Marks)

(Compulsory Question: It should be a Case study/Application oriented/Critical analysis from any of the units)

(Q.No: 10)

QUESTION PAPER PATTERN FOR MODEL / END SEMESTER EXAM

Reg.No:---------- Q.P.CODE:

HINDUSTHAN COLLEGE OF ARTS & SCIENCE (AUTONOMOUS)

PG/MBA/MCA DEGREE MODEL EXAMINATIONS ----------20--------

(----------Semester)

BRANCH: ----------

Subject Name: ----------

Time: Three Hours **Maximum: 60 Marks**

SECTION – A (5x4=20 marks)

Answer **ALL** Questions

ALL Questions carry **EQUAL** Marks

(Q.No 1 to 5 Either Or type)

(One question from each Unit)

SECTION – B (3x10=30 Marks)

Answer any **THREE** Questions Out of **FIVE** Questions

ALL Questions carry **EQUAL** Marks

(Q.No 6 to 10)

(One question from each Unit)

SECTION – C (1x10=10Marks)

(Compulsory Question: It should be a Case study/Application oriented/Critical analysis from any of the units)

(Q.No: 11)

Blue Print of Question Paper for all PG Programmes

(For the academic year 2021-22, 2022-23)

FOR CIA I - QUESTION PATTERN — **Max. Marks:50**

Sec	Question No	Type	No of Question	Questions to be answered	Mark per question	K-level
A	1 to 4	Either or Type (a or b)	8	4	4 (4x4=16)	2 Questions will be in K1 4 Questions will be in K2 2 Questions will be in K3
B	5 to 9	Open choice	5	3	8 (3x8=24)	2 Questions will be in K3 2 Questions will be in K4 1 Questions will be in K5
C	10	Compulsory	1	1	10 (1x10=10)	1 Question will be in K5

FOR MODEL/ESE - QUESTION PATTERN — **Max. Marks:60**

Sec	Question No	Type	No of Questions	Questions to be answered	Mark per question	K-level
A	1 to 5	Either or Type (a or b)	10	5	4 (5x4=20)	2 Questions will be in K1 4 Questions will be in K2 4 Questions will be in K3
B	6 to 10	Open choice	5	3	10 (3x10=30)	2 Questions will be in K3 2 Questions will be in K4 1 Questions will be in K5
C	11	Compulsory	1	1	1 (1x10=10)	1 Question will be in K5

Distribution of section-wise marks with K levels for PG 2021-22, 2022-23

CIA - PG								
Sec.	K1	K2	K3	K4	K5	Total questions	Questions to be answered	Total marks
A- Either or type	2	4	2			8	4	4X4=16
B - Open choice			2	2	1	5	3	3X8=24
C- Compulsory Question					1	1	1	1X10=10
Total Marks	8	16	16	16	18			84
% of marks without choice	9.52	19.05	19.05	119.05	21.43			100

Model Exam - PG								
Sec.	K1	K2	K3	K4	K5	Total questions	Questions to be answered	Total marks
A- Either or type	2	4	4			10	5	5X4=20
B - Either or type			2	2	1	5	3	3X10=30
C – Compulsory Question					1	1	1	1X10=10
Total Marks	8	16	36	20	20			100
% of marks without choice	8	16	36	20	20			100

PG Programme Regulations for the academic year 2022-2023

1. Internal marks components for all the candidates admitted from the academic year 2022-2023 and onwards is as follows.

For Theory courses

Components	Marks
Test	15
Model Exam	15
Internal Assessment components	20
TOTAL	50

For Practical courses

Components	Marks
Test –I	15
Test – II	15
Observation/Excercise	10
Application*	10
TOTAL	50

2. Pattern of question paper for External Examination will be maximum of 60 marks for all theory courses. The marks obtained will be converted into 50 marks as per the scheme.
3. Passing minimum marks for all PG programme is 50 % in internal and 50% in External and the composition of total 50 marks out of 100 marks.
4. Project work is considered as a special course involving application of knowledge in problem solving / analyzing /exploring a real-life situation. A Project work may be given in lieu of a discipline specific elective paper. Distribution of marks for major project work for all PG Programmes will be of 50:50 pattern for both Internal and External in total of 200 marks.
5. Internship / Institutional Training / Mini-Project/ Extension Activity is related to the discipline. The students can be permitted to complete the Internship / Institutional Training / Mini-Project/ Extension Activity before the end of respective semesters (end of I, II and III semester) and submit a report.

Internship / Institutional Training/ Extension Activity	Not more than seven days
Mini project	During the course of study for not more than seven days.

6. For fully internal subjects, Two test will be conducted one at the time of CIA I and the other will be during Model Examinations.
7. Retest for the failure candidates in the above case should be conducted immediately before the End Semester Examinations.
8. For the Theory cum Practical blended courses, 50:50 Internal and External pattern will be followed for theory examination and Fully internal pattern will be followed for Practical examination. For theory part, External examination will be conducted as regular pattern (max of 70 marks) and it will be converted into 25 marks.

Course	Internal Marks		External marks		Total marks (Max. marks 50)	
	Min.	Max.	Min.	Max.	Min.	Max.
Theory	12.5	25	12.5	25	25	50
Practical	25	50	-		25	50

For Practical components for Theory cum Practical courses (Fully Internal)

Components	Marks
Test I	10
Test II	10
Experiment/Exercise	20
Record	5
Viva	5
Total	**50**

The Internal mark 50 will be converted into 25.

11. For the candidates admitted under the Fast Track System (FTS) must register their names to their concerned department heads and get approval from the COE office at the beginning of the II semester.

12. Self Study will be a Core Paper of the department for which the examination pattern of other theory subjects is followed.

13. Online courses is incorporated as a non-credit skill enhancement course for the III and IV semesters and Grades will be assessed based on the certificates produced by the students. It is compulsory to produce one online course certificate for each semester to avail grades for the students. (2 certificates in any of the online platform is mandatory).

14. SDR – Student Development Report to be received by the department from the students till end of the **Third** semester. (Evidences of Curriculum activities and Co-curriculum activities).

15. Open elective courses:

Departments can offer list of subjects which teaches moral ethics to the young community for the better future. The topics relevant to Indian ethics, Culture, Women rights, Yoga, Green farming, Indian constitution etc., as an open elective courses. These courses can be offered by the department or other department as inter department courses. Marks earned for this subject will not be included for the CGPA calculation.

Regulations of Fast Track System (FTS)

- From the academic year 2021-22, our college is offering Fast Track System (FTS) for all UG and PG programmes. In this system, we are offering two courses under the course type of Discipline Specific Elective (DSE) in the sixth semester for all UG programmes and fourth semester for all PG programmes, which are equivalent and related with **National Programme on Technology Enhanced Learning/Study Webs of Active-Learning for Young Aspiring Minds** (NPTEL/SWAYAM) courses.

- The students have the option of taking two subjects of the sixth semester of their programme through NPTEL/SWAYAM portal from the list given by NPTEL and can complete the online course before fifth semester and submit the received original certificates to the COE office for getting approval. If the student completes these courses before the beginning of the sixth semester (UG)/fourth semester (PG), the candidate can be considered and exempted to write the examination from the assigned DSE courses in the sixth semester/fourth semester. They should complete only the self study course and project work during the VI/IV semester as assigned in the scheme. The candidate who completes the online courses and submits the successful course completion credentials, the credit transfer will be considered as per our Scheme of Examination for qualifying the degree. **The minimum duration of the registered online course must be 12 weeks.** Course duration of less than 12 weeks will not be considered.

- For all PG programmes, the candidates who were admitted during the academic year 2021-2022 under the Fast track system, for the self study course, the internal mark component will be as follows. For others regular internal pattern follows.

TEST	Max. Marks	Mode
CIA I	50 (50x1=50)	Online objective type
Model Exam.	50 (50x1=50)	Online objective type

Out of these two tests, the total marks will be converted into 40 marks as Internal.

- For all UG programmes, the candidates who were admitted during the academic year 2021-2022 under the Fast track system, for the self study course, the internal mark component will be as follows. For others regular internal pattern follows.

TEST	Max. Marks	Mode
CIA I	50 (50x1=50)	Online objective type
CIA II	50 (50x1=50)	Online objective type
Model Exam.	50 (50x1=50)	Online objective type

Out of three tests, the total mark will be converted into 30 marks as Internal.

- For the students admitted in Fast Track System, must enroll their names to the concerned department heads and get approval from the COE office at the beginning of III semester for all UG Programmes and at the beginning of II semester for all PG programmes.

- The students who cleared and got certified for online courses under the fast track system, the grade obtained will be converted into average marks of range. The received certificates must be submitted to the COE office for approval of the Controller and the Principal. The FTS courses will be treated as fully external.

DEPARTMENT OF ELECTRONICS				CLASS: M.Sc ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
I	DSC	22ELP01	Digital and Network Communication	4	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	✓
	Entrepreneurship Oriented	
	Skill Development	✓

Course Objectives

1. Students can be able to understand the building blocks of digital communication system.
2. Able to understand the network architecture and protocols.
3. Students can get exposure and implement on various modulation schemes.
4. Can able to analyze different types of protocols used in network architecture.
5. Can able to evaluate transmission techniques in communication related jobs.

Unit	Course Contents	Hours	K Level
I	**Signal Digitization** Sampling Theorem – Pulse Amplitude Modulation – Pulse Position Modulation –Pulse Width Modulation – Pulse Code Modulation – Quantization: Quantization Noise – Delta Modulation: Adaptive Delta Modulation –Signal Power – Signal to Quantization Noise Ratio–PCM and DM Voice Signal Comparison–Time Division Multiplexing – CCITT.	13	Up to K5
II	**Digital Radio** Digital Radio Block Diagram – Digital Modulation: Amplitude Shift Keying –Frequency Shift Keying – Phase Shift Keying – Binary Phase Shift Keying –Quadrature Phase Shift Keying– Quadrature Amplitude Modulation– Digital Demodulation: Coherent Demodulation–Coherent Detection– FSK Demodulator– MFSK Receivers–BPSK Demodulator– QPSK Demodulation–QAM Demodulation.	13	Up to K5
III	**Data Communication** Introduction–Basic Terms and Concepts–Line Configurations– Topology– Transmission Media–MODEM: Standard and Types–Analog and Digital transmission: Encoding and Modulating–Channel Capacity–Base Band and Broad Band– Transmission Impairments–Multiplexing: FDM–TDM–Error Detection and Control: CRC.	13	Up to K5
IV	**Network Architecture and Protocols** Layered Architecture – OSI model – Functions of Layers – Data Link Control Protocols – ARQ – Stop and Wait – Sliding Window – Go back and Selective Repeat– Asynchronous Protocol: X Modem–Y Modem–Kermit– Synchronous Protocol: BSC– SDLC–HDLC– TCP/ IP Model–SMTP– HTTP –FTP.	13	Up to K5

V	**LAN and ISDN** LAN: Standard, Protocol - Infrared LAN– IEEE 802 Standards: ETHERNET – LLC – MAC –CSMA/CD–Token Ring–Token Bus–FDDI–ALOHA–SONET–ISDN: IDN – Channels – User Interfaces – ISDN Layers – Broad Band ISDN – Frame Relay–ATM: Concept and Architecture– ISDN Protocol–Physical Layer Protocol–D–channel Data Link Layer–Layer 3 Protocols–Network Signaling Systems:SS7 Protocol.	13	Up to K5

Note: The Questions should be asked in the ratio of Theoretical concept 90% and Problem solving 10%

Book for Study

1. Harold Kolimbiris, "**Digital Communication Systems with Satellite and Fiber Optics Applications**", Pearson Education, Third Indian Reprint, 2004. (Unit–I to V)

Books for Reference

1. JohnG.Proakis, "**Digital Communications**", McGraw–Hill Higher Education, fourth edition, 2009
2. Behrous. A.Forouzan, "**Data Communication and Networking**", Tata McGrawHill, fourth Edition, 2000.
3. Sanjay Sharma, "**Communication Systems**", S.K. Kataria & Sons, first edition.
4. Forouzan, "**Data Communications and Networking**" , 5th Edition, Paperback – 1 July 2017
5. Michael Moher Simon Haykin, "**An Introduction to Analog & Digital Communications**", 2ed Paperback –2012

Web Resources

1. https://nptel.ac.in/courses/106/105/106105082/
2. https://nptel.ac.in/courses/117/101/117101051/

Pedagogy: Chalk & Talk, Exercise, Assignments & PPTs.

Rationale for Nature of the Course: Digital and network communication opens to the digitized fast growing world

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Dr. R. Prema

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K – Level
CLO 1	Conclude the performance of PAM, PCM and DM in a digital communication	Up to K5
CLO 2	Evaluate the different types of digital modulations chimes for implementing digital radio	Up to K5
CLO 3	Reframe the concept of analog and digital transmission techniques.	Up to K5
CLO 4	Analyze different types Network Architecture and Protocols	Up to K5
CLO 5	Evaluate the working of LAN and ISDN	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CLO 1	3	3	3	3	3	3	3
CLO 2	2	3	3	2	2	3	2
CLO 3	3	3	2	3	3	2	3
CLO 4	3	2	3	2	3	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Dr. R. Prema	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
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Hindusthan College of Arts & Science
Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: M.SC ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
I	DSC	22ELP02	Microwave and RADAR Navigation System	4	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	✓
	Entrepreneurship Oriented	
	Skill Development	✓

Course Objectives

1. To enable the students to learn the operations of wave equation.
2. To get deep knowledge in Microwave Devices and Circuits.
3. To get thorough knowledge about uses of microwave amplifiers and oscillators.
4. Can get exposure on wave guides and microwave antennas.
5. To enable the students to know more about RADAR systems.

Unit	Course Contents	Hours	K Level
I	**EM Wave Theory** Introduction to Microwaves: History–Region and Band Designations–Advantages–Applications–Maxwell'sEquations:Ampere'sLaw–Faraday's Law–Gauss Law–Wave Equations–TEM/TE/TM/HE Wave Definitions –Transmission Lines - Two wire parallel transmission lines –Voltage and current relationship on transmission lines.	13	Up to K5
II	**Microwave Devices** Classification of Solid-State Microwave Devices – Varactor Diodes – PIN Diode– Schottky Barrier Diode (SBD)– Tunnel Diode–Gunn Diode–Photo Diode - IMPATT Diode– TRAPATT Diode–BARITT Diodes – Quantum Electronic Devices.	13	Up to K5
III	**Microwave Amplifiers and Oscillators** Klystrons: Two Cavity Klystron Amplifier–Multicavity Klystron–Reflex Klystron–Traveling Wave Tube (TWT): Construction–Operation–Backward Wave Oscillator– Magnetrons: Cavity Magnetron Operation–Sustained Oscillations in Magnetron– Applications.	13	Up to K5
IV	**Waveguides and Microwave Antennas** Types of Waveguides– Propagation of Waves in Rectangular Waveguides–TE and TM Modes–Propagation of TM Waves in Rectangular Waveguide–TM Modes in Rectangular Waveguides. **Horn Antenna:** Sectoral E & H–plane Horn– Pyramidal Horn and Conical Horn – Parabolic Reflector: Feed for Parabolic Reflector – Lens Antenna –Slot Antenna–Micro Strip Antenna: Operation–Methods of Analysis– Polarization–Dual frequency.	13	Up to K5

V	RADAR Block Diagram – Classification: Doppler – Pulsed – Free Space RADAR Range Equation – Maximum Unambiguous Range –RADAR Receivers –Modulators – RADAR Displays: Plan Position Indicator (PPI) – Doppler Effect – CW Doppler RADAR – Moving Target Indicator (MTI) RADAR–Frequency Modulated CWRADAR–Radio Navigational Aids: Long Range Navigational Aid (LORAN).	13	Up to K5

Note: The Questions should be asked in the ratio of Theoretical concept 80% and Problem solving 20%

Book for Study

1. Dr.Kulkarni.M, **"Microwave and Radar Engineering "**, Umesh Publications, Fifth Revised Edition, 2015. (Unit–I to V)

Books for Reference

1. Merrill I. Skolnik, **"Introduction to RADAR Systems"**, Tata McGraw–Hill, Third Edition, Fifth Reprint, 2002.
2. David M. Pozar. **"Microwave Engineering"**, Wiley Publications, fourth edition.
3. Merrill I. Skolnik, **"Introduction to Radar Systems"**, McGraw Hill Book Company, Second edition.
4. Sharma K. K., **"Fundamentals of Microwave and Radar Engineering"**, Paperback, ISBN: 9788121935371, 9788121935371.
5. Merrill Skolnik, **"Introduction To Radar Systems"**, Paperback – 1 July 2017

Web Resources

1. https://nptel.ac.in/courses/108/103/108103141/
2. https://nptel.ac.in/courses/108/105/108105154/

Pedagogy: Chalk & Talk, Exercise, Assignments & PPTs.

Rationale for Nature of the Course: Microwave communication is the back bone of terrestrial communication and also the sole of mobile communication

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Ms. Mahitha Mohan

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K – Level
CLO 1	Evaluate and recognize Maxwell's Equations	Up to K5
CLO 2	Summarize the working of various microwave devices	Up to K5
CLO 3	Estimate the working of microwave amplifiers and oscillators	Up to K5
CLO 4	Criticize the performance of wave guides and various antennas	Up to K5
CLO 5	Predict the working of RADAR system and its applications	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO**	**PO 6**	**PO 7**
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	3	3	2	3	3	2	3
CLO 4	3	2	3	2	2	3	3
CLO 5	2	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Ms. Mahitha Mohan	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
Department of Electronics
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Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS					CLASS: M.Sc ECS		
Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
DSC	22ELP03	8051 Microcontroller with C Programming	4	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	
	Entrepreneurship Oriented	✓
	Skill Development	

Course Objectives

1. To enable the Students to learn the architecture and instruction sets.
2. To express the concepts of programming and Interfacing concepts of 8051Microcontroller.
3. To understand the assembly and C language programs.
4. Able to use interrupts and serial communication concepts.
5. Can evaluate the programming concepts for real time applications.

Unit	Course Contents	Hours	K Level
I	**Overview of 8051** Microcontrollers and Embedded Processors – Overview of 8051 Family –8051Architecture –Timers –Registers and Memory Organizations.	13	Up to K5
II	**8051AssemblyLanguage Programming** Inside the 8051–Pin Out–Instruction Set: Addressing Modes–Data Transfer Instruction–Logical Instruction–Arithmetic Instructions–Jump and Call Instructions –Bit Oriented Instructions –Flags and Stack.	13	Up to K5
III	**Programming with C** Data Types - Directives –Time Delay Programming – I/O Programming – Logic Operations – Arithmetic Operations – Timer Programming – Counter Programming.	13	Up to K5
IV	**8051Interrupts & Peripherals** 8051 Interrupts – Programming Timer Interrupts Programming External Hardware Interrupts – 8051 Serial Communication Programming–Programming with Serial Communication Interrupts –Peripheral and Interrupt Programming in C.	13	Up to K5
V	**Real World Applications and Case Studies** LCD Interfacing–Keyboard Interfacing–Parallel and Serial ADC Interfacing – DAC Interfacing – Sensor Interfacing and Signal Conditioning – 8051 C Programming for the 8255 – Accessing external data memory in 8051 - RTC Interfacing – Relays and Opto – Isolator Interfacing–Stepper Motor Interfacing – DC Motor Interfacing and PWM.	13	Up to K5

Note: The Questions should be asked in the ratio of Theoretical concept 90% and Problem solving 10%

Book for Study

1. Muhammad Ali Mazidi, JaniceGillispie Mazidiand Rolin D.Mc Kinlay, "**The 8051 Microcontroller and Embedded Systems Using Assembly and C**" by PHI, 2nd Edition, 2006.(Unit–I toV)

Books for Reference

1. *Kenneth J.Ayala, "**The 8051 Microcontroller**",Delmar Cengage Learning, 3rd Edition, 2004.*
2. *SubrataGhoshal, "**8051 Microcontroller:Internals, Instructions, Programming and Interfacing**", Pearson Education, second edition, 2014.*
3. *Kenneth Ayala, "**The 8051 Microcontroller**", 3rd Edition (English, Paperback, Kenneth Ayala), 2007.*
4. *V Udayashankara, M Mallikarjunaswamy, "8051 MICROCONTROLLER: HARDWARE, SOFTWARE & APPLICATIONS", Paperback – 1 July 2017.*
5. *Reema Thareja, "**Programming in C**", Paperback – 25 February 2016.*

Web Resources

1. https://nptel.ac.in/courses/108/105/108105102/
2. https://nptel.ac.in/courses/117/104/117104072/

Pedagogy: Chalk & Talk, Exercise, Assignments & PPTs.

Rationale for Nature of the Course: It is the embedded software which primarily governs the functioning of embedded systems.

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Dr. M. Kumaresan

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Rate the fundamentals of microprocessors and architecture of 8051	Up to K5
CLO 2	Summarize the assembly and C language programs of 8051	Up to K5
CLO 3	Conclude the function of interrupts and serial communication in real world applications	Up to K5
CLO 4	Discriminate different types of external interfaces including LEDS, LCD, Keypad, Matrix, Switches & Seven segment display.	Up to K5
CLO 5	Evaluate programming concepts of real time applications	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	PO 1	PO 2	PO 3	PO 4	PO	PO 6	PO 7
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	2	3	2
CLO 3	3	3	2	3	3	2	3
CLO 4	2	2	3	2	3	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Dr. M.Kumaresan	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
Department of Electronics
Hindusthan College of Arts & Science
Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: I M.Sc ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
I	DSC	22ELP04	Power Electronics	4	4	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	✓
	Entrepreneurship Oriented	
	Skill Development	✓

Course Objectives

1. To impart the knowledge of different types of Power Semiconductor Devices
2. To get exposure on switching characteristics and applications.
3. To enable the students to work with static switches and voltage controllers.
4. Can able to design inverters and power supplies and become an entrepreneur.
5. Able to get thorough knowledge about regulators.

Unit	Course Contents	Hours	K Level
I	**Power Electronic Devices** Introduction–Power Semiconductor Devices: Power Diodes–Power Transistors: Power MOSFET – Insulated Gate Bipolar Transistor (IGBT) –Thyristors: SCR, DIAC, TRIAC – Other Power Electronic Devices: SIT– MCT–PUT–SCS–SUS–GTO–SITH.	11	Up to K5
II	**Controlled Rectifiers** Controlled Rectifiers: Phase Controlled Converter–Single–Phase Semi Converter– Single– Phase Series Converter– Three phase converters - DC Choppers: Step Down Operation: Step Down with RL Load–Step Up Operation–Switch Mode Regulator: Buck Regulator – Boost Regulator – Buck–Boost Regulator –CUK Regulator.	11	Up to K5
III	**Static Switches & AC Voltage Controllers** AC Switches: Single Phase– Three Phase– Three Phase Reversing Switches–AC Switches for Bus Transfer–DC Switches– Solid State Relays – AC Voltage Controller: ON–OFF Control –Phase Control – Single Phase Bidirectional Controllers: Resistive Loads – Inductive Loads– Cyclo Converters: Single Phase Cyclo Converters.	10	Up to K5
IV	**Inverters** Single Phase Bridge Inverters –Three Phase Inverters–Voltage Control: Single PWM– Multiple PWM–Sinusoidal PWM– Phase Displacement Control– 60–Degree PWM – Third–Harmonic PWM.	10	Up to K5

V	**Power Supplies** DC Power Supplies: Switched Mode – Resonant – Bidirectional – AC Power Supplies: Switched Mode – Resonant – Bidirectional – UPS – Static Circuit Breakers- Battery Charger–Emergency Lighting System.	10	Up to K5

Note: The Questions should be asked in the ratio of Theoretical concept 90% and Problem solving 10%

Book for Study

1. Rashid.M.H,"**Power Electronics circuits, Devices and Applications**", Third Edition, Prentice Hall, 2018.(Unit–I to V)

Books for Reference

1. V. Jagannathan, **Power Electronics: Devices and Circuits**, PHI Publications, Second Edition, 2013
2. Dr.Bimbhra.P.S,"**PowerElectronics**",KhannaPublishers,FifthEdition,2014.
3. V. Vijayendran, "**Introduction to Integrated Electronics: Digital and Analog**",

   S. Printers & Publishers, 2009. (Unit: 3 to 5)
3. D. Pleach, A.P. Malvino and G. Saha, "**Digital Principles and Applications**", Tata McGraw- Hill Education PvtLtd, NewDelhi, 6th Edition, 2009.
4. J. Millman &C.C. Halkias, "**Electronic Devices and Circuits**", Tata McGrawHill, NewDelhi, 1985.

Web Resources

1. https://nptel.ac.in/courses/108/108/108108111/
2. https://nptel.ac.in/courses/108/102/108102145/

Pedagogy: Chalk & Talk, Exercise, Assignments & PPTs.

Rationale for Nature of the Course:- *Power Electronics* signifies the word *power electronics* and control or we can say the electronic that deal with power equipment for power control.

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Dr. K. Thangavel

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Summarize the fundamental concepts of power electronic devices such as SCR, TRIAC and Power MOSFET etc.	Up to K5
CLO 2	Evaluate the working of controlled rectifiers and regulators.	Up to K5
CLO 3	Estimate the working of static switches and voltage controllers	Up to K5
CLO 4	Judge the ability to characterize inverters and power supplies for industrial needs.	Up to K5
CLO 5	Predict the design concept of UPS, battery charger, emergency lighting system etc.,	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	3	3	2	3	3	2	3
CLO 4	3	2	3	2	3	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Dr. K. Thangavel	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
Department of Electronics
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Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
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Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: M.Sc ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
I	DSC	22ELP05	Practical I - Digital Communication Systems	3	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	
	Entrepreneurship Oriented	
	Skill Development	✓

COURSE OBJECTIVES

1. To impart the knowledge on implementation of baseband modulation techniques.
2. To enable the students to work on various modulation technologies.
3. Can able to design different types of modulation process.
4. Able to get thorough knowledge about delta modulation and demodulation techniques.
5. Get exposure on designing of quadrature modulation and demodulation schemes.

Experiment No.	Topics (Any 10 Experiments)	Hours	K Level
1	PAM Generation and Detection	5 Hours	Up to K5
2	PWM Generation and Detection	5 Hours	Up to K5
3	PPM Generation and Detection	5 Hours	Up to K5
4	Frequency Sampling	5 Hours	Up to K5
5	Pulse Code Modulation and Demodulation	5 Hours	Up to K5
6	Linear Pulse Code Modulation and Demodulation	5 Hours	Up to K5
7	ASK Generation and Detection	5 Hours	Up to K5
8	FSK Generation and Detection	5 Hours	Up to K5
9	PSK Generation and Detection	5 Hours	Up to K5
10	QPSK Generation and Detection	5 Hours	Up to K5
11	DPSK Generation and Detection	5 Hours	Up to K5
12	BPSK Generation and Detection	5 Hours	Up to K5

13	QAM Generation and Detection	5 Hours	Up to K5
14	Delta Modulation and Demodulation	5 Hours	Up to K5
15	Adaptive Delta Modulation and Demodulation	5 Hours	Up to K5

Book for Study

1. Harold Kolimbiris, "**Digital Communication Systems with Satellite and Fiber Optics Applications**", Pearson Education, Third Indian Reprint, 2004.

Books for Reference

1. John G. Proakis,"**Digita lCommunications**",McGraw–Hill Higher Education, fourth Edition, 2000.
2. ***Simon Haykin, " Communication Systems",*** 4TH EDITION. ***Simon Haykin***. McMaster University. JOHN WILEY & SONS, INC. New York & Chichester.
3. Michael Moher Simon Haykin "An Introduction to Analog & Digital Communications", 2ed Paperback – 1 January 2012.
4. Simon Haykin , "Digital Communications" Paperback – 1 January 2006
5. *Dr. J. S. Chitode, Dr. Balasaheb H. Patil, Dr.D.G. Bhalke, "Digital Communications", 1st Edition*

Web Resources

1. https://nptel.ac.in/courses/108/104/108104098/
2. https://nptel.ac.in/courses/117/101/117101051/

Pedagogy: Practical Demonstration

Rationale for Nature of the Course:- This *course* is intended to develop the skills to diagnose and rectify the errors occur in ***Digital communication system.***

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Dr. R. Prema

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Estimate the implementation of baseband modulation techniques	K1
CLO 2	Conclude the PCM and DM concept to design digital communication system	Up to K2
CLO 3	Apprize the working of various pulse modulation schemes	Up to K3
CLO 4	Predict various digital modulators and demodulators for implementing digital communication	Up to K4
CLO 5	Evaluate the output characteristics of quadrature modulation and demodulation process.	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	3	3	2	3	3	2	3
CLO 4	3	2	3	2	3	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Dr. R. Prema	Name & Signature Dr. K. Thangavel	Name & Signature

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Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

Sem	DEPARTMENT OF ELECTRONICS						CLASS: M.Sc ECS
I	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
	DSC	22ELP06	Practical II - 8051Microcontroller And its Applications	3	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	✓
	Entrepreneurship Oriented	
	Skill Development	

COURSE OBJECTIVES

1. To impart the outline of the practical skills for developing own ALP.
2. To understand C program for real world applications using8051 microcontrollers.
3. Can able to design various embedded system products.
4. Able to distinguish between various code converters.
5. Get exposure to interpret the designing of programs based on real time applications.

Experiment No.	Topics (Any 10 Experiments)	Hours	K Level
1	Arithmetic and Logic Operations	5 Hours	Up to K5
2	Data Transfer with Parallel Port	5 Hours	Up to K5
3	PWM Generation	5 Hours	Up to K5
4	Solid State Relay Interface using Interrupt	5 Hours	Up to K5
5	Interfacing Matrix Keypad	5 Hours	Up to K5
6	Seven Segment Display Interface	5 Hours	Up to K5
7	LCD Interface	5 Hours	Up to K5
8	Data Transfer with Parallel Port	5 Hours	Up to K5
9	DAC Interface	5 Hours	Up to K5
10	ADC Interface	5 Hours	Up to K5
11	Stepper Motor Interface	5 Hours	Up to K5
12	Serial Communication Interface	5 Hours	Up to K5
13	Digital Clock	5 Hours	Up to K5
14	Traffic Light Controller	5 Hours	Up to K5
15	Water Level Controller	5 Hours	Up to K5

Book for Study

1. Muhammad Ali Mazidi, JaniceGillispie Mazidiand Rolin D.Mc Kinlay, "**The 8051 Microcontroller and Embedded Systems Using Assembly and C**" by PHI, 2nd Edition, 2006.

Books for Reference

1. Kenneth J.Ayala,"**The 8051 Microcontroller**",Delmar Cengage Learning, 3rd Edition, 2004.
2. SubrataGhoshal, "**8051 Microcontroller:Internals, Instructions, Programming and Interfacing**", Pearson Education, second edition, 2014.
3. Kenneth Ayala, "**The 8051 Microcontroller**", 3rd Edition (English, Paperback, Kenneth Ayala), 2007.
4. V Udayashankara, M Mallikarjunaswamy, "**8051 MICROCONTROLLER: HARDWARE, SOFTWARE & APPLICATIONS** ", Paperback – 1 July 2017.
5. Reema Thareja, "**Programming in C**", Paperback – 25 February 2016.

Web Resources

1. https://nptel.ac.in/courses/106/108/106108100/
2. https://nptel.ac.in/courses/108/105/108105102/

Pedagogy: Practical demonstration

Rationale for Nature of the Course:- *8051 Microcontroller* is well-suitable for students those who want to know about embedded systems. Since, it is the most popular microcontroller used in embedded system.

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Dr. M. Kumaresan

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Estimate and apply basic programming concepts of 8051μC	Up to K5
CLO 2	Summarize the data transfer operation through serial and parallel ports	Up to K5
CLO 3	Conclude the ADC&DAC interfacing with 8051μC	Up to K5
CLO 4	Evaluate various embedded System products to solve real time problems using 8051μC	Up to K5
CLO 5	Justify the programming concepts of Traffic light and water level controller	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	PO 1	PO 2	PO 3	PO 4	PO	PO 6	PO 7
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	3	3	2	3	3	2	3
CLO 4	3	2	3	2	3	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Dr. M. Kumaresan	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
Department of Electronics
Hindusthan College of Arts & Science
Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: M.Sc ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
II	DSC	22ELP08	Optical Fiber Communication	4	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	
	Entrepreneurship Oriented	
	Skill Development	✓

Course Objectives

1. To facilitate the knowledge about Optical Fiber Fabrication,
2. To understand the characteristics of Optical Sources & detectors
3. To determine the signal distortion and bending loss of signals.
4. To impart knowledge on Optical sources and detectors.
5. To get strong knowledge in Optical Networks and applications.

Unit	Course Contents	Hours	K Level
I	**Optical Fiber Fabrication** Motivation for Light Wave Communications – Optical Spectral Bands – Nature of Light–Basic Optical Laws–Fiber Materials–Fiber Fabrication: Classification – Chemical Vapor Deposition – Modified chemical vapor deposition (MCVD), outside vapor deposition (OVD), and vapor axial deposition (VAD) Multi–Element Glasses –Phasil System Comparisons of Various Fabrication Processes Drawing and Coating–Double Crucible Method–Rod–In Tube Method–Mechanical Properties.	13	Up to K5
II	**Optical Fibers and their Properties** Basic Structure of Optical Fiber Conditions for Total Internal Reflection–Principles of light propagation – Types of fibers: Step Index & Graded Index fibers–Modes of Propagation: Single and Multimode–Calculation of Acceptance Angle –Numerical Aperture–Advantages and Application.	13	Up to K5
III	**Signal Degradation** Attenuation – Absorption – Scattering & Bending losses – Core & Cladding losses – Signal distortion in Fibers – Modal Delay – Factors contributing to dispersion – Group delay – Material & Waveguide dispersion – Signal distortion in Single Mode Fibers – Polarization mode dispersion – Characteristics of single mode fiber – Cut-off wavelength – Mode – Field Diameter – Single mode fiber bending loss–Dispersion power penalty–Total dispersion delay–Maximum Transmission rate–Dispersion shifted Fiber.	13	Up to K5
IV	**Light Sources and Photo Detectors** Light Sources: LED – Fiber LED Coupling – LASERS–Operation types – Spatial Emission–Current v/s output characteristics. Photo Detectors: Characteristics– Photo Emissive Type–Photo Conductive–Photo Voltaic Devices–PIN Photodiode – Avalanche Photo Diode.	13	Up to K5

V	**Optical Networks &Applications** Wave Length Division Multiplexing – Dense WLDM – Digital Subscriber Line Technology – SONET/SDH: SONET Network Layers –Frame Format– SONET Multiplexing – SONET Topologies – SDH – Community Antenna Television (CATV)–Special Applications: Digital Video Transmission Using Optical Fibers networks receiver–High performance receiver– Design of fiber optic receiver– Fiber based MODEMS.	13	Up to K5

Note: The Questions should be asked in the ratio of Theoretical concept 90% and Problem solving 10%

Book for Study

1. Gerd Keiser, "**Optical Fiber Communications**", Tata McGraw Hill Publications, Fifth Edition, 2017.

   (Unit–I to V)

Books for Reference

1. Robert J Schoenbeck "**Electronic Communications Modulation and Transmission**", PHI,1999.
2. Optical Fiber Communications: Principles and Practice, Pearson Education, Third Edition, 2010.
3. Gerd Keiser, **"Optical Fiber Communication"**, 5th Edition Paperback – 1 July 2017
4. John M. Senior, **"Optical Fiber Communications: Principles and Practice"** - Principles and Practice 3 Edition, English, Paperback, 2010
5. **MYNBAEV, "Fiber-Optics Communications Technology"**, 1e Paperback – 1 January 2002.

Web Resources

1. https://nptel.ac.in/courses/108/104/108104113/
2. https://nptel.ac.in/courses/117/101/117101054/

Pedagogy: Chalk & Talk, Exercise, Assignments & PPTs.

Rationale for Nature of the Course:- The proposed *course* aims to expose the students to the basics of *optical fiber communication* system including signal propagation through *optical fibers.*

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Ms. Mahitha Mohan

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Conclude the fabrication process of optical fibers	Up to K5
CLO 2	Distinguish the types of optical fibers	Up to K5
CLO 3	Argue the characteristics of single mode fibers	Up to K5
CLO 4	Apprise the function of various light sources and detectors	Up to K5
CLO 5	Evaluate the performance of optical fibers in SONET, CATV and SDH etc.	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	**PO 1**	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	2	3	2	3	3	2	3
CLO 4	3	2	3	2	2	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Ms. Mahitha Mohan	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
Department of Electronics
Hindusthan College of Arts & Science
Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: M.Sc ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
II	DSC	22ELP09	MEMS and Control Systems	4	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	✓
	Entrepreneurship Oriented	✓
	Skill Development	✓

Course Objectives

1. To learn the concept of MEMS and micro systems.
2. To impart knowledge on Control systems and thermal systems.
3. To correlate and apply the same in open and closed loop systems.
4. To differentiate time and frequency domain responses.
5. Evaluate the working characteristics of PID controllers.

Unit	Course Contents	Hours	K Level
I	**Overview of MEMS & Micro System** MEMS & Microsystems- typical MEMS & Micro system products– Evaluation of Micro fabrication – Microsystems and Microelectronics – The Multidisciplinary nature of Micro Systems design and Manufacture – Micro Systems and miniaturization – applications of Micro Systems in Auto motive industry– applications of Microsystems in other industries.	13	Up to K5
II	**Working Principles of Microsystems** Micro sensors – Micro actuation using Thermal Forces – Actuation Using shape memory Alloys – Actuation Using Piezoelectric crystals – Actuation using Electro static forces–MEMS with Micro Actuators–Micro Accelerometers– Micro Fluidies.	13	Up to K5
III	**Concepts of Control Systems** Introduction to control systems-Human elements in control systems- block diagram fundamentals- open loop control system-closed loop control systems-Linear and Nonlinear Systems- Effect of feedback on Overall gain, Stability, Sensitivity and Noise-Physical system representation: Electrical Systems and thermal system.	13	Up to K5
IV	**Block Diagrams, Signal Flow Graphs and Time Response Analysis** Introduction to Block Diagrams - Block diagram reduction-Signal flow graph - Signal flow graph algebra construction of signal flow graph from block diagram - Mason's gain formula-Time Response Analysis of First and second Order systems - Steady state error.	13	Up to K5

V	**Stability Analysis, Compensation and Controllers** Stability Analysis of Control System: Bode plot- Routh Hurwitz criterion-Root Locus-Nyquist Criterion-Principles of P-PI-PD-PID Controllers-Cascade and feedback compensation, lag, lead, lag-lead Compensation.	13	Up to K5

Note: The Questions should be asked in the ratio of Theoretical concept 90% and Problem solving 10%

Book for Study

1. TaiRanHsu, **"MEMS & Microsystems Design and Manufacture"**– Tata Mc Graw Hill. (Unit I to V)

Books for Reference

1. Katsuhiko Ogata **"Modern Control Engineering"**. Pearson Education Asia, Fourth edition, 2002.
2. Benjamin C.Kuo"**Automatic Control Systems**", PHI,1995.
3. S.N.Verma, "**Automatic Control Systems**",Khanna Publishers. (UnitIII)
4. A.NagoorKani,**"ControlSystems"**,RBAPublications.(UnitIV&V)
5. Sergey Edward Lyshevski, **"MEMS and NEMS: Systems, Devices, and Structures"**, (Nano- and Microscience, Engineering, Technology and Medicine) Hardcover – 1 January 2002

Web Resources

1. https://nptel.ac.in/courses/117/105/117105082/
2. https://nptel.ac.in/courses/108/101/108101037/

Pedagogy: Chalk & Talk, Exercise, Assignments & PPTs.

Rationale for Nature of the Course:- Because of the large surface area to volume ratio of ***MEMS***, forces produced by ambient electromagnetism

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Dr. M. Kumaresan

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Rate the concepts of MEMS and Microsystems	Up to K5
CLO 2	Summarize the fundamentals of control systems	Up to K5
CLO 3	Reframe the concept of control system in electrical and thermal systems	Up to K5
CLO 4	Consider the time and frequency-domain responses of first and second-order systems	Up to K5
CLO 5	Evaluate the stability analysis of control systems and controllers.	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	2	3	2	3	3	2	3
CLO 4	3	2	3	2	3	3	3
CLO 5	2	3	2	3	2	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Dr. M. Kumaresan	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
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Hindusthan College of Arts & Science
Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: M.Sc ECS				
Sem	**Course Type**	**Course Code**	**Course Title**	**Credits**	**Contact Hours / Week**	**CIA**	**Ext**	**Total**
II	DSC	22ELP10	Embedded Systems and RTOS	4	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	
	Entrepreneurship Oriented	✓
	Skill Development	✓

Course Objectives

1. To enable the students to recall the basics of RTOS
2. To become familiar with PIC microcontroller in embedded systems.
3. To get thorough knowledge on peripheral devices of PIC microcontrollers.
4. To understand architecture of embedded systems and services.
5. To know more about real time operating systems and applications.

Unit	Course Contents	Hours	K Level
I	**Embedded Systems** Definition and Classification– Overview of Embedded Controllers–Exemplary High Performance Processors – CISC and RISC Architecture–Hardware Unit in an Embedded System– Software Embedded into a System – Structural units in a processor – Direct Memory Access – Device Drivers.	13	Up to K5
II	**PIC16F877 Architecture and Instruction Set** Device Overview– Architecture– Memory Organization– Status Register– Option Register– INTCON Register– PCON Register– I/O Ports– Data EEPROM – Instruction Set: Byte Oriented Operations – Bit Oriented Operations–Literal and Control Operations.	13	Up to K5
III	**PIC Peripheral Features** TIMER 0 Module–TIMER 1 Module– TIMER 2 Module– Capture/ Compare/ PWM Modules – I^2C transmission and reception – USART – ADC Module –Special features of the CPU: Oscillator Selection–Power on Reset–Power up Timer – Oscillator Startup Timer–Brown out Reset–Interrupts– Watchdog Timer–SLEEP.	13	Up to K5
IV	**Embedded Software Architecture &Operating System Services** Round Robin–Round Robin with Interrupts– Function Queue Scheduling Architecture– Real Time Operating Systems (RTOS)– Tasks and Data– Semaphores and Shared Data– Message Queues, Mail Box and Pipes–Timer Function – Events– Memory Management.	13	Up to K5

V	**Real Time Operating Systems** Study of Micro C/OS–II – Vx Works – Other Popular RTOS – RTOS System Level Functions– Task Service Functions– Time Delay Functions– Memory Allocation Related Functions– Semaphore Related Functions– Mailbox Related Functions – Queue Related Functions – Case Studies of Programming with RTOS: Case Definition, Multiple Tasks and their Functions– Creating a list of Tasks, Functions and IPCs–Exemplary Coding Steps.	13	Up to K5

Note: The Questions should be asked in the ratio of Theoretical concept 90% and Problem solving 10%

Book for Study

1. Rajkamal, "**Embedded Systems Architecture, Programming and Design**", TATAMcGraw–Hill, Second Edition, 2008. (Unit I to V)

Books for Reference

1.ShibuKV, "**Introduction to Embedded System**" Tata McGraw Hill, 2010.

2.MicroCOS II Reference Manual, Salvo User Manual & VX works Programmers Manual.

3.Martin.P.Bates,"**Programming 8–bit PIC Microcontrollers in C Interactive Hardware Simulation**" Elsevier, Second Edition, 2008. (Unit II& III)

4.PIC16f877ADataSheet.

5.David E. Simon, "**An Embedded Software Primer**", Addison Wesley, Ninth Impression, 2011.(Unit IV& V)

Web Resources

1. https://nptel.ac.in/courses/108/102/108102045/
2. https://nptel.ac.in/courses/108/105/108105057/

Pedagogy: Chalk & Talk, Exercise, Assignments & PPTs.

Rationale for Nature of the Course: This *course* teaches *embedded system* design using a building block approach, which allows one to visualize the requirement of an *embedded system*

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: S. Sathyadeepa

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Conclude the fundamentals of Embedded system	Up to K5
CLO 2	Support to get the knowledge in RTOS	Up to K5
CLO 3	Apply the functions of RTOS through case studies	Up to K5
CLO 4	Find System Design using PIC Microcontrollers	Up to K5
CLO 5	Evaluate real time operating system functions	UP to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	3	3	2	3	3	2	3
CLO 4	3	2	3	2	3	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Mrs. S. Sathyadeepa	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
Department of Electronics
Hindusthan College of Arts & Science
Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: M. Sc ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
II	DSC	22ELP11	Modern VLSI Design	4	4	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	✓
	Entrepreneurship Oriented	✓
	Skill Development	✓

Course Objectives

1. To equip the students to learn about fabrication of active and passive components
2. Can able to design the process of VLSI circuit.
3. Can able to impart implementation of programmable logic devices.
4. To enable the students to get knowledge on design methodologies of ASIC.
5. Can able to evaluate VLSI design approaches.

Unit	Course Contents	Hours	K Level
I	**VLSI Fabrication Technology** History of VLSI – Fabrication: MOSFET – Wafer Manufacture – Wafer Cleaning – Doping and Impurities Addition – Growth & Deposition of Dielectric Films – Masking and Lithography– Etching and Metallization – Packing – Fabrication of Passive Components – Process Flow for CMOS Fabrication – Twin Tub Process.	11	Up to K5
II	**VLSI Design Flow** VLSI Circuit Design Process – Design Flow – Architecture Specification and Design Constraints – HDL Capture and RTL Coding – Logic Simulation – Logic Synthesis – Logic Optimization – Formal Verification– Static Timing Analysis– Floor Planning – Placement& Routing – Layout Vs Schematic – Design Rule Check.	11	Up to K5
III	**Programming Logic Devices** Programmable Logic Array (PLA) – Programmable Array Logic (PAL) – Implementation Approaches in VLSI Design – Custom or Full Custom Design– Semicustom Design – Gate Arrays – Complex Programmable Logic Devices (CPLD) – CPLD Architectures..	10	Up to K5
IV	**Issues in Chip Design** Requirements of Chip Design – System On Chip (SOC) – Chips Power Consumption – Clock – Chip Reliability – Analog Integration in the Digital Environment – CAD Systems – Layout Analysis – Case Study.	10	Up to K5

V	**ASIC Design** Chip Design – Design Methodologies: IBM ASICs– HP7100LC – Wiper Digital Video Chip – Kitchen Timer Chip: Specification and Architecture – Logic and Layout Design – Validation – Microprocessor Data Path: Clocking and Bus Design.	10	Up to K5

Note: The Questions should be asked in the ratio of Theoretical concept 90% and Problem solving 10%

Book for Study

1. K. Llal Kishore, V.S.V. Prabhakar,"**VLSI DESIGN**"I.K International Publishing House, 2009. (Unit-I to V)

Books for Reference

1. Bhaskar.J,"**VHDLPrimer**",PHI, Low price Edition, 2001.
2. Douglas L. Perry, "**VHDL Programming by Example**" Tata Mc-Graw-Hill, Fourth Edition, 2002.
3. Wayne Wolf, "***Modern VLSI Design***", Pearson Education, 3rd Edition, 1997
4. Yuan Taur & Tak H. Ning "**Fundamentals of Modern Vlsi Devices**" Second Edition by, CAMBRIDGE INDIA
5. Yuan Taur, Tak H. Ning, "**Fundamentals of Modern VLSI Devices**" **Feb 10, 2022.**

Web Resources

1. https://archive.nptel.ac.in/courses/108/101/108101089/
2. https://nptel.ac.in/courses/108/107/108107129/

Pedagogy : Chalk & Talk, Exercise, Assignments & PPTs.

Rationale for Nature of the Course:- The **course** aims to provide students a thorough understanding of the fundamental concepts and **design** of **VLSI** systems

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: S. Sathyadeepa

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Evaluate fabrication of passive and active electronics Components.	Up to K5
CLO 2	Compare the VLSI design flow and VLSI circuit design process.	Up to K5
CLO 3	Reframe the design flow of programmable logic devices.	Up to K5
CLO 4	Conclude the chip design issues and demonstrate the various design applications using ASIC.	Up to K5
CLO 5	Summarize the VLSI based system design for various applications	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	3	3	2	3	3	2	3
CLO 4	2	2	3	2	3	3	3
CLO 5	3	3	3	3	M	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Mrs. S. Sathyadeepa	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
Department of Electronics
Hindusthan College of Arts & Science
Coimbatore-641 028

Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: M. Sc ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
II	DSC	22ELP12	Practical III - Optical and Microwave Communication	3	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	✓
	Entrepreneurship Oriented	✓
	Skill Development	

COURSE OBJECTIVE

1. To impart the knowledge of establishing optical and microwave communication.
2. To get familiar with bending and coupling losses occur in fibers.
3. To get strong knowledge about characteristics of reflex klystron and gunn diode oscillator.
4. To understand the performance of microwave components.
5. To evaluate the characteristics of microwave devices.

Experiment No.	Topics (Any 10 Experiments)	Hours	K Level
1	Study of Fiber Optic Trainer	5 Hours	Up to K5
2	Establishment of Analog Fiber Optic Link	5 Hours	Up to K5
3	Establishment of Digital Fiber Optic Link	5 Hours	Up to K5
4	Measurement of Attenuation Loss	5 Hours	Up to K5
5	Measurement of Bending Loss	5 Hours	Up to K5
6	Measurement of Coupling Loss	5 Hours	Up to K5
7	Study of Microwave Components and Instruments	5 Hours	Up to K5
8	Reflex Klystron Characteristics	5 Hours	Up to K5
9	Frequency Measurement of Reflex Klystron	5 Hours	Up to K5
10	VSWR Measurement	5 Hours	Up to K5
11	Attenuator Characteristics	5 Hours	Up to K5
12	Study of Gunn Diode Oscillator	5 Hours	Up to K5
13	Measurement of Unknown Load Impedance	5 Hours	Up to K5

14	Isolator and Circulator Characteristics	5 Hours	Up to K5
15	Horn Antenna Characteristics	5 Hours	Up to K5

Book for Study

1. Gerd Keiser, "**Optical Fiber Communications**", Tata McGraw Hill Publications, Fifth Edition, 2017.

Books for Reference

1. Robert J Schoenbeck "**Electronic Communications Modulation and Transmission**", PHI,1999.
2. Optical Fiber Communications: Principles and Practice, Pearson Education, Third Edition, 2010.
3. Gerd Keiser, **"Optical Fiber Communication "**, 5th Edition Paperback – 1 July 2017
4. John M. Senior, **"Optical Fiber Communications : Principles and Practice"** - Principles and Practice Edition, English, Paperback, 2010
5. **MYNBAEV, "Fibre-Optics Communications Technology"**, 1e Paperback – 1 January 2002

Web Resources

1. https://nptel.ac.in/courses/108/104/108104113/
2. https://nptel.ac.in/courses/117/101/117101054/

Pedagogy : Practical Demonstration

Rationale for Nature of the Course:- The proposed **course** aims to expose the students to the basics of **optical fiber communication** system including signal propagation through **optical fibers**

Activities to be given

1. Assignment on Linear space and group theory.
2. Preparing the students to appear professional courses by giving advanced exercise and work out problems and to go with real time applications.
3. Prepare for Collaborative working.

Name of the Course Designer: Ms. Mahitha Mohan

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Distinguish the working of analog and digital optical communication system	Up to K5
CLO 2	Compare the Attenuation, Bending and Coupling Loss of optical fibers	Up to K5
CLO 3	Grade the characteristics of Reflex Klystron and Gunn Diode Oscillator	Up to K5
CLO 4	Predict the performance of various microwave components	Up to K5
CLO 5	Evaluate the working of microwave devices	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	3	3	2	3	2	3	3
CLO 4	3	2	3	2	3	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Ms. Mahitha Mohan	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
Department of Electronics
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Co-ordinator
Curriculum Development Cell
Hindusthan College of Arts & Science,
Coimbatore-641 028.

DEPARTMENT OF ELECTRONICS				CLASS: M. Sc ECS				
Sem	Course Type	Course Code	Course Title	Credits	Contact Hours / Week	CIA	Ext	Total
II	DSC	22ELP13	Practical IV- Embedded System and RTOS	3	5	50	50	100

Nature of Course		
Knowledge and Skill Oriented	Employability Oriented	✓
	Entrepreneurship Oriented	
	Skill Development	✓

Course Objectives

1. To impart the knowledge of developing own embedded systems for various applications.
2. To understand the interfacing concept of various peripherals.
3. To know the design concepts on seven segment display.
4. To get familiar with DAC and ADC converters.
5. Can able to program with stepper motor and other interfacing concepts.

Unit	Course Contents (Any 10 Experiments)	Hours	K Level
1	Delay Generation using Timer	Hours	K Level
2	PWM Generation	5 Hours	Up to K5
3	LED Interfacing and Object Counter	5 Hours	Up to K5
4	Interfacing Solid State Relay	5 Hours	Up to K5
5	Interfacing Seven Segment Display	5 Hours	Up to K5
6	LCD Interface	5 Hours	Up to K5
7	DAC Interface	5 Hours	Up to K5
8	Internal ADC Programming	5 Hours	Up to K5
9	External Event Counter using Timer–1	5 Hours	Up to K5
10	Programming using interrupts	5 Hours	Up to K5
11	Serial Port Interfacing Using RS232	5 Hours	Up to K5
12	Water Level Controller	5 Hours	Up to K5
13	Stepper Motor Interface	5 Hours	Up to K5
14	RTOS Multitasking	5 Hours	Up to K5

Book for Study

1. Rajkamal, "**Embedded Systems Architecture, Programming and Design**", TATA McGraw–Hill, Second Edition, 2008.

Books for Reference

1. Shibu K V,"**Introduction to Embedded System**"TataMcGrawHill,2010.
2. MicroCOS II Reference Manual, Salvo User Manual & VX works Programmers Manual.
3. Martin.P.Bates,"**Programming8–bit PIC Microcontrollers in C Interactive Hardware Simulation**", Elsevier, Second Edition, 2008. (Unit II& III)
4. PIC16f877A Data Sheet.
5. David E. Simon, "**An Embedded Software Primer**", Addison Wesley, Ninth Impression, 2011.

Web Resources

1. https://nptel.ac.in/courses/108/102/108102045/
2. https://nptel.ac.in/courses/108/105/108105057/

Pedagogy: Practical demonstration

Name of the Course Designer: Mrs. S. Sathyadeepa

Course Learning Outcomes

CLOs	On Completion of the Course, the students should be able to	K - Level
CLO 1	Evaluate and apply basic programming concepts	Up to K5
CLO 2	Summarize the interfacing concept of various peripherals with embedded microcontroller	Up to K5
CLO 3	Estimate the data transfer information through serial and parallel ports	Up to K5
CLO 4	Predict various real world applications of Embedded Systems	Up to K5
CLO 5	Evaluate stepper motor and traffic light control	Up to K5

Mapping of Course Learning Outcomes (CLOs) with Programme Outcomes (POs)

	Programme Outcomes (with Graduate Attributes)						
CLOs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CLO 1	3	3	3	3	3	3	3
CLO 2	3	3	3	3	3	3	2
CLO 3	3	3	2	3	2	3	3
CLO 4	3	2	3	2	3	3	3
CLO 5	3	3	3	3	3	3	3

3 – Advance Application 2 – Intermediate Level 1 – Basic Level

Course Designed by	Verified by HOD	Approved by CDC Coordinator
Name & Signature of the Staff Mrs. S. Sathyadeepa	Name & Signature Dr. K. Thangavel	Name & Signature

Head of the Department
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Co-ordinator
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